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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,038	08/19/2004	Wen-Koi Lai	NAUP0577USA	5037

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EXAMINER
SMITH, BRADLEY

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,038	LAI ET AL.	
	Examiner	Art Unit	
	Bradley K. Smith	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8,9,14* is/are rejected.

7)☒ Claim(s) *6,7 and 10-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *search notes*.

DETAILED ACTION

Election/Restrictions

Applicant's election of group I in the reply filed on 10/27/06 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 8, 9 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Nanjo et al. (US Patent 6,900,088). Nanjo et al. disclose providing a substrate, at least one first gate structure and at least one second gate structure being included on a surface of the substrate, both the first gate structure and the second gate structure having sidewalls; performing a first ion implantation process to form a shallow-junction

doping region of a first conductive type in the substrate next to each of the sidewalls of the first gate structure; forming offset spaces on each of the sidewalls of the first gate structure and the second gate structure; and performing a second ion implantation process to form a shallow-junction doping region of a second conductive type in the substrate next to the offset spacer on each of the sidewalls of the second gate structure (see figures 6A-6H and columns 16 and 17). With regards to claim 2, Nanjo et al. disclose the substrate is silicon. With regards to claim 3, Nanjo et al. disclose the first and second gate structures comprise a gate dielectric and polysilicon gate electrodes (406c). With regards to claim 4, Nanjo et al. disclose the first dopant of the implant process is arsenic and the first gate structure is a gate of an NMOS (column 16 lines 55-60). With regards to claim 5, Nanjo et al. disclose forming a dielectric layer on the surface of the substrate to cover the first gate structure and the second gate structure; and performing a dry etching process to vertically remove the dielectric layer down to the surface of the substrate (column 16 lines 30-50). With regards to claim 8, Nanjo et al. disclose the second dopant ion is boron and for a PMOS structure. With regards to claim 9, Nanjo et al. disclose forming a sidewall on a third gate structure at the same time as the formation of the sidewalls on the first and second gate structures (see figure 8C). With regards to claim 14, since Nanjo et al. disclose the same process and claim 14 adds no new method steps it would be inherent that Nanjo et al. process would perform the same function.

Allowable Subject Matter

Claims 6, 7, and 10-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record neither teaches nor reasonably suggests the formation of TEOS by LPCVD at a temperature of 650 to 680 deg C (claims 6 and 7), forming a spacer layer on the surface of the substrate to cover the first gate structure, the second gate structure, the third gate structure; and the offset spacers on each of the sidewalls of the first gate structure, the second gate structure, and the third gate structure; and performing an etching process to form a spacer at sides of the first gate structure, the second gate structure, and the third gate structure (claim 10 and 13), further comprising at least one third ion implantation process after performing the second ion implantation process to form a lightly doped drain region in the substrate next to the offset spacer on each of the sidewalls of the third gate structure (claim 11) further comprising at least one pocket ion implantation process after performing the second ion implantation process to form a pocket doping region in the substrate at either side of the first gate structure, the second gate structure, and the third gate structure (claim 12).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bradley K. Smith whose telephone number is 571-272-1884. The examiner can normally be reached on 10-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Bradley K Smith
Primary Examiner
Art Unit 2891